Analysis and Design of a Single Stage Single Switch Power Factor Corrected Converter

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A power converter is used as an interface between utility and most of the power electronic equipments. Since these converters draw pulsed current from the supply, which is high in third and fifth harmonic content, line current harmonics are injected to the electrical network which hampers Power Quality. To improve input current quality, Power factor corrected converter (PFC) has been widely employed in industry. The reduction of current harmonics using various PFC techniques is investigated and related to the EN 61000-3-2 standard. A major problem associated with Single Stage Single Switch Switch Mode Rectifier is strong dependency of DC bus voltage stress across the capacitor with the output load. Power unbalance between PFC stage and DC-DC stage is the inherent reason for causing high DC bus voltage stress. Existing single stage ac-dc converter with harmonic free input current are costly and require either complex control circuit or and/or more component power circuit to minimize dc bus voltage stress. Introduced here is a design method where no additional component is required to suppress the dc bus voltage.

This paper derives a design solution for achieving low voltage stress and unity power factor, in a single stage single switch converter by optimally selecting the boost inductance using Equal Area Criterion (EAC) and using fast acting proportional controller. The converter consists of a Discontinuous Conduction Mode (DCM) boost converter cascaded with a Continuous Conduction Mode (CCM) fly back converter, fast voltage regulation is achieved by simple PWM control. The performance of the converter with the proportional controller has been verified. The limiting duty ratio for the normal operation of the proposed converter is 0.5. It is observed that by proper selection of the inductance using EAC and with the simple proportional controller, the DC bus voltage at light load is found to be completely eliminated. The proposed converter has a simpler power circuit and simpler control circuit, has less component count, and it does not contribute to any additional voltage stress. The analysis of the implemented circuit and the design procedure are presented. The experimental result shows that voltage across the bus capacitor is kept under 230V for full range operation (90-270V) and load (20-80W). The maximum power factor is 0.995 and the maximum efficiency is 90 %. For cost sensitive application this converter may be preferred. This converter can be considered to be a better alternative for power quality improvement because of reduced size of overall converter, higher efficiency, lower cost, and enhanced reliability compared to other means of power quality improvement. The effect of load variation on the proposed converter was also studied to demonstrate and validate its performance. According to the results, the THD of the ac mains current lies between 9.5% and 8.3% in the complete range of varying loads, with a nearly unity power factor operation.

**Key words:** Power Factor Improvement, AC-DC converter, Power Quality, Equal Area Criterion (EAC)

1. Introduction

Many methods have been proposed in the literature to minimize the harmonics in the line current. A conventional method of solving the harmonic current in the power supply is the power factor correction circuit. It is well known that DCM (Discontinuous Conduction Mode) Boost converter has an inherent PFC (Power Factor Correction) function with constant duty cycle control. Integration of Boost converter with CCM (Continuous Current Mode) dc-dc converter is able to achieve input current wave shaping and output voltage regulation. The energy storage element is required to buffer the difference between instantaneous input power and the instantaneous output power. Fast voltage regulation is achieved by simple PWM (Pulsed Width modulation) control. Many different power converter topologies have been proposed that integrates functions of PFC and isolated dc-dc conversion in a single stage. Computer and its peripherals require power supply that are capable of operating in 90-265V range and can provide holdup time 10 ms, the required energy to support the output during the holdup time is obtained from properly sized energy storage capacitor.

The main disadvantage of single stage approach is the unregulated dc bus voltage which varies with line and load. [1], [2]. Power unbalance between PFC stage and output stage is the reason for high dc bus voltage stress. The value of dc bus capacitor is quite crucial as it affect the response, cost, stability and efficiency. Due to the general desire to reduce converter size, weight and cost, it is necessary to reduce dc bus voltage stress.[3]-[6]

Existing previous work have been analysed. The topology [2] proposes the integrated PFC converter with power stage negative feedback. [7] Proposes the controller circuit for the single stage single switch PFC regulator. The control circuit is too complex with more component count. The topology [8] proposes a single stage single switch converter by modulating the predetermined frequency of the converter to reduce bus voltage stress. The topology [9] proposes boost/fly back single stage single switch power factor corrected converter with low loss snubber.[10] proposes single stage single switch bi-fly back converter. Even though the topologies shown in [2],[8]-[11]...
proposes a solution to this problem, they have disadvantage of more component count in the power circuit. [12] shows a topology that can only be used for non-isolated applications. In this paper a design method is proposed to avoid the problem of energy unbalance by optimally sizing the boost inductor and making the dc bus voltage independent of the load condition. This can be achieved by equating the absorbed power from the line to the delivered power to the load within a half line cycle. Which implies, voltage across energy storage capacitor:

\[ V_{dc} = V_{in} \sqrt{\frac{1}{L_1}} \]  

(1)

Now the voltage stress depends upon the ratio of two magnetizing inductance and is proportional to the input voltage, it is independent of the load condition. By properly designing the value of the two inductors high voltage stress can be reduced.

2. Proposed Converter

The proposed converter is the integration of DCM Boost converter and CCM Fly back converter. The energy storage capacitor \( C_1 \) is connected in series path of energy flow. Controller used is a proportional controller. Selection of component is very important to achieve specified performance. With a small value of boost inductor large switching ripples are injected into the supply current, and large value of it does not allow shaping the ac mains current. The input power is controlled only by duty cycle and boost inductance. Small value of capacitor results in large ripple in steady state and big dip and rise in dc link voltage under transient condition. There are continuous attempt to reduce the size and cost of new configuration. High frequency transformer design is very important to reduce size, cost and losses. Voltage controller, comparator are implemented using Op-amp based analog circuit. Converter uses only single switch for input current wave shaping and output voltage regulation.

Equal area criterion (EAC) is applied to achieve optimum design of boost inductor, coupled with a closed loop control with output dc voltage as controlled variable and duty ratio as manipulated variable so as to eliminate the problem of dc bus voltage stress at light load. The operation of the converter is as follows:

When the switch S turns on, causing the current in inductor \( L_1 \) to ramp up from zero with a slope, this is proportional to the instantaneous line voltage. Diode D is reversed biased. At the end of this interval the amount of energy is stored in \( L_1 \) which depends only on input line voltage and is independent of the current and voltages of other inductors and capacitors.

When S turns off, which causes the current in inductor \( L_1 \), to ramp down with a slope proportional to the instantaneous line voltage minus the energy storage capacitor voltage \( V_{dc} \) minus the output voltage reflected to the primary. Diode D conducts.

3. EAC applied to design of boost inductor for the proposed single stage single switch power factor converter[13]

A typical input current pulse superimposed on the reference current \( I_{m} \sin \omega t \), is shown in Image. 2. EAC applied to single stage single switch power factor converter means equalizing the area under a sinusoidal reference current and the area under the input current in the total period of one switching cycle [14].

The value of this inductor is quite crucial in the performance of the converter with the small value of this inductor the large switching ripples are injected into supply current, and large value of it doesn’t allow shaping the AC mains current in the desired fashion. Therefore the optimum selection of this inductor is essential to achieve satisfactory performance[15]

Design Basis:
1. Assuming zero switching loss
2. Required power output is obtained at a low turn ON time or duty ratio (0.26), by this varying power levels can be achieved under DCM.

3. Find out value of input peak current during turn ON such that area under reference input current in one switching period made equal to the area under the current pulse as shown in Image. 2

4. Switching instance is considered as $\alpha = 90^\circ$ for the maximum rising and falling slope at the peak of input voltage.

Design of the output converter is usual fly-back converter design. Fly back transformer is designed so that it serves the dual role of inductor and transformer.[16]

*Implementation:*

A 100 w experimental prototype has been built with the following specification:
- $L_1 = 1.57 \text{ mH}$, $C_1 = 116 \mu\text{F}$, $n=3.5$, $C_2 = 317\mu\text{F}$, $T_s=50\text{ns}$, $D=0.26$, $R = 25\Omega$,
- $L_{\text{core}} = \text{E42/21/15}$, Transformer core = E65/32/13, Transformer $L_2=1.2 \text{ mH}$,
- Limiting duty ratio for DCM operation is 0.5. Switch $S$ used is IRFPF50.

4. **Simulation And Experimental Results**

   ![Image 7 Experimental result showing Input Voltage and Input current](image7.png)

   ![Image 8 Simulation result showing input current](image8.png)

   ![Image 9 Experimental result showing dc bus voltage stress and input voltage](image9.png)

   ![Image 10 output power and dc bus voltage stress](image10.png)

   ![Image 11 Harmonic analysis](image11.png)

   ![Image 12 Input line voltage and Power factor](image12.png)
Image 7 and Image 8 show that the converter can provide nearly unity power factor. Image 9 reveals no dc bus voltage stress for the load variation. Image 10 shows the measured voltage stress on the storage capacitor against output power which confirms the effectiveness of the stress control. The proposed converter can keep the capacitor voltage stress between 217-230v for a change of loading form full load to one-tenth load. Image 11 shows that the proposed converter can provide sufficient margin in harmonic current reduction for complying the standard EN 61000-3-2. The measured THD of the converter varies from 8.3%-9.5%, which indicates a very high input power factor as shown in Image 12.

8. Conclusion

This paper derives a design method for achieving near unity power factor, low voltage stress and fast output voltage regulation in a single stage ac-dc converter. Control is extremely simplified using conventional PWM (Pulse Width Modulation) circuitry. The performance of the converter has been verified with experimental test. The measured overall efficiency is 90%. The technical advantage of the proposed converter is a design method for reducing the voltage stress. Low cost, compared to additional magnetic component of other solution in the literature. Proposed converter can provide sufficient margin in harmonic current reduction for complying the standard EN 61000-3-2.

References


